I CLAIM:

1. An integrated circuit comprising testing circuitry and core logic circuitry, comprising:

a memory that stores data identifying analog nodes in the core logic circuitry and tolerance values associated with the analog nodes;

a condition checker that compares actual test values of the analog nodes with the associated tolerance values; and

a main control unit coupled to the memory and the condition checker that synchronizes testing of the core logic circuitry.

2. The integrated circuit of claim 1 wherein the testing circuitry enables analog testing for on-line, off-line, and interactive field testing.

3. The integrated circuit of claim 1 wherein the testing circuitry further comprises a tester interface.

4. The integrated circuit of claim 3 wherein the tester interface is a host computer interface.

5. The integrated circuit of claim 1 wherein the testing circuitry further comprises a second memory for storing diagnostic data.

6. The integrated circuit of claim 1 wherein the memory is located in the testing circuitry or one of the embedded memories in the core logic circuitry.

7. The integrated circuit of claim 1 wherein the memory is a programmable memory.

8. The integrated circuit of claim 1 wherein the testing circuitry is JTAG-compliant.

9. The integrated circuit of claim 1 wherein the testing circuitry includes a test controller module comprising:

a memory for storing data transmitted to the test controller module;

a control unit; and

a test access port controller.

10. The integrated circuit of claim 1 wherein the testing circuitry further comprises a second test controller module.

11. The integrated circuit of claim 1 wherein the condition checker comprises:

means for receiving the test values from the analog nodes

means for receiving the associated tolerance values; and

means for checking whether the test values are within the associated tolerance values.

12. The integrated circuit of claim 11 wherein the condition checker further comprises noise calibration circuitry.

13. The integrated circuit of claim 1 wherein the testing circuitry further comprises a second condition checker.

14. The integrated circuit of claim 1 wherein the main control unit comprises:

a program counter;

a plurality of registers for storing addresses of analog nodes; and

a control unit.

15. The integrated circuit of claim 14 wherein the main control unit further comprises:

a data pointer for addressing a memory to archive test results.

16. The integrated circuit of claim 14, wherein the testing circuitry comprises a plurality of condition checkers, and wherein the main control unit further comprises:

means for selecting a condition checker from the plurality of condition checkers in the testing circuitry to compare a test value with an associated tolerance value.

17. A method for testing an integrated circuit having multiple analog nodes and testing circuitry, comprising:

selecting an analog node in the integrated circuit from a list of analog nodes stored in a memory;

obtaining a test value from the selected analog node;

retrieving a tolerance value associated with the selected analog node from a memory; and

comparing the test value of the selected analog node with the tolerance value.

18. The method of claim 17 wherein the associated tolerance value is retrieved from the same memory in which the list of analog nodes is stored.

19. The method of claim 17, wherein the comparing comprises checking whether the test value of the selected analog node is within the associated tolerance value.

20. The method of claim 19 further comprising generating an error indication signal in response to the checking.

21. The method of claim 20 further comprising:

reconfiguring a memory in the integrated circuit to be operable to store diagnostic data from the testing circuitry.

22. The method of claim 21 further comprising:

storing data identifying the selected analog node in the memory; and

storing the test value of the selected analog circuit in the memory.

23. The method of claim 20 further comprising:

storing data identifying the selected analog node in a data memory in the testing circuitry; and

storing the test value of the selected analog circuit in a data memory in the testing circuitry.

24. The method of claim 23 wherein the data identifying the selected analog node and the test value of the selected analog circuit are stored in the same data memory.

25. The method of claim 24 further comprising:

obtaining a test value of a second analog node, wherein the second analog node is associated with the selected analog node;

storing data identifying the second analog node in the data memory; and

storing the test value of the second analog node in the data memory.

26. The method of claim 24 further comprising uploading the contents of the data memory to a host computer.

27. The method of claim 17 wherein the obtaining is responsive to stimuli transmitted to the integrated circuit from a location outside the integrated circuit.

28. The method of claim 17 further comprising:

prior to the comparing, selecting a condition checker in the testing circuitry for performing the comparing.

29. The method of claim 17 further comprising, prior to the selecting:

storing data identifying the analog nodes of the integrated circuit in a program memory in the testing circuitry;

storing tolerance values associated with the analog nodes of the integrated circuit in the program memory.

30. An integrated circuit comprising testing circuitry and core logic circuitry, wherein the testing circuitry comprises:

means for selecting an analog node in the core logic circuitry from a list of analog nodes stored in a memory;

means for obtaining a test value from the selected analog node;

means for retrieving a tolerance value associated with the selected analog node from a memory; and

means for checking whether the test value of the selected analog node is within the associated tolerance value.

31. The integrated circuit of claim 30 wherein the means for checking comprises a means for generating an error indication signal in response to the checking.

32. The integrated circuit of claim 30 further comprising:

a means for storing data identifying the selected analog node in a data memory; and

a means for storing the test value of the selected analog node in a data memory.

33. The integrated circuit of claim 30 further comprising a means for communicating with a host computer.

34. The integrated circuit of claim 30 further comprising:

a means for selecting a condition checker for performing the comparing.

35. A method for testing an integrated circuit having multiple analog nodes and testing circuitry, the method comprising:

selecting an analog node in the integrated circuit from a list of analog nodes stored in a memory in the testing circuitry;

obtaining a test value from the selected analog node;

retrieving a tolerance value associated with the selected analog node from a memory in the testing circuitry; and

comparing the test value of the selected analog node with the tolerance value; wherein the selected analog circuit is of a type selected from the group including at least: an analog-to-digital converter, a digital-to-analog converter, and a filter.

36. A computer-implemented method, comprising:

transmitting instructions for generating testing circuitry which includes:

instructions for selecting an analog node from a list of analog nodes stored in a memory of an integrated circuit;

obtaining a test value from the selected analog node;

retrieving a tolerance value associated with the selected analog node from a memory; and

comparing the test value of the selected analog node with the tolerance value.